AMENDMENT UNDER 37 C.F.R. § 1.111
U.S. Patent Application No. 09/762,233

AMENDMENTS TO THE SPECIFICATION

Page 13, please replace the heading on line 7 as follows:

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"~~DISCLOSING~~ SUMMARY OF THE INVENTION"

Page 21, please insert the following paragraphs after the third full paragraph:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram of a LC display coupled to driving devices.

FIG. 2 is chart showing voltage-brightness behavior of a display element.

FIG. 3 is a chart showing voltage-brightness behavior of the display element.

FIG. 4 is a timing diagram of the driving voltages and cell voltages corresponding to a method without pulse-length modulation.

FIG. 5 is a timing diagram of the driving voltages and cell voltages corresponding to a method with pulse-length modulation.

FIG. 6 is a timing diagram of the cell voltage amplitude and the corresponding timing diagrams of the stationary oscillation of the cell quasi-rms voltage.

FIG. 7 is a cell voltage timing diagram.

FIG. 8 is a timing diagram of the driving voltages and cell voltages.

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FIG. 9 is a timing diagram of the driving voltages and cell voltages.

FIG. 10 is a timing diagram of the driving voltages corresponding to a method without pulse-length modulation.

FIG. 11 is at timing diagram of driving voltages for signal electrodes corresponding to a method with pulse-length modulation.

FIG. 12 is a timing diagram of row driving voltages for four-line addressing.

FIG. 13 is a diagram of matrices of row driving voltages for four-line addressing.

FIG. 14 is a diagram of Static square voltage - brightness behavior of a display element (without regard to the "frame response").

FIG. 15 is a diagram of dynamic square voltage - brightness behavior of a display element (with regard to the "frame response").

FIG. 16 is a timing diagram for the one-line addressing corresponding to the first embodiment.

FIG. 17 is a timing diagram for the two-line addressing corresponding to the first and eleventh embodiments.

FIG. 18 is a timing diagram for the one-line addressing corresponding to the first, second, and third embodiments.

FIG. 19 is a timing diagram for the two-line addressing corresponding to the first, second, third, and eleventh embodiments.

A2 FIG. 20 is a timing diagram for the two-line addressing corresponding to the first, second, third, fourth, and fifth embodiments.

FIG. 21 is a timing diagram of pulse shifts for three groups of signal electrodes corresponding to the sixth and third embodiments.

FIG. 22 is a timing diagram of pulse shifts for three groups of signal electrodes corresponding to the sixth and fifth embodiments.

FIG. 23 is a block diagram of the display driving device.

FIG. 24 is an output circuit diagram of the seventh embodiment.

FIG. 25 is an output circuit diagram of the seventh embodiment with the additional transistors for adjusting output resistance.

FIG. 26 is a timing diagram corresponding to the eighth embodiment.

FIG. 27 is a timing diagrams corresponding to the ninth embodiment.

FIG. 28 is a diagram showing the shapes of voltage pulses corresponding to the tenth embodiment.

FIG. 29 is a timing diagram corresponding to the eleventh embodiment with pulse-length modulation.

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Please delete the paragraphs at page 53, line 29 through page 55, line 17.

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Please delete the present Abstract of the Disclosure and replace it with the following new Abstract of the Disclosure.

Method addressing LCDs and apparatus drastic decreasing cross-talks and uniformity on high frame frequencies to achieve high contrast are disclosed. During ~~the~~ selection period T_r, display column electrodes receive two additional identical voltage levels ~~whose polarities are symmetric~~ of opposite polarities about the reference voltage V_0, the levels allocated to the boundary portions of the period T_r, and the third additional V_0-level of constant duration applying between the voltage levels of opposite polarities. ~~The additional opposite polarity levels allocated to the boundary portions of the period T_r.~~ All levels are applied to the column electrode in direct or in reverse order. The allocation of the levels alternates in succeeding periods T_r, on adjacent column electrodes, in succeeding frame periods. The voltage pulses to column electrodes are split into ~~a~~ groups being related to different electrodes and shifted in time. The shifting times are changed in the course of time ~~(Fig.21)~~. The driving device incorporates output block which output resistances for different voltage levels have the same values. The display electrodes receive ~~a~~ compensation voltages ~~that are~~ independent of image patterns. The pulse shapes provide self-compensation of spurious changes of ~~the~~ mean square voltages ~~on LC cells. For the two line addressing mode, column driving voltages have the informational and quasi-reference equalizing components. Row and column driving voltages are set equal to $|V_{s0}|\sqrt{1-\eta}$ and $|V_{s0}|\sqrt{1+\eta}$, where η is an the voltage adjustment parameter. N_{max} of the display is no less than N_{max0} determined for a particular voltage timing diagram. All embodiments of the invention are complement each other. The aim is to improve drastic the image uniformity and contrast, and to increase of the display size and operation speed.~~

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